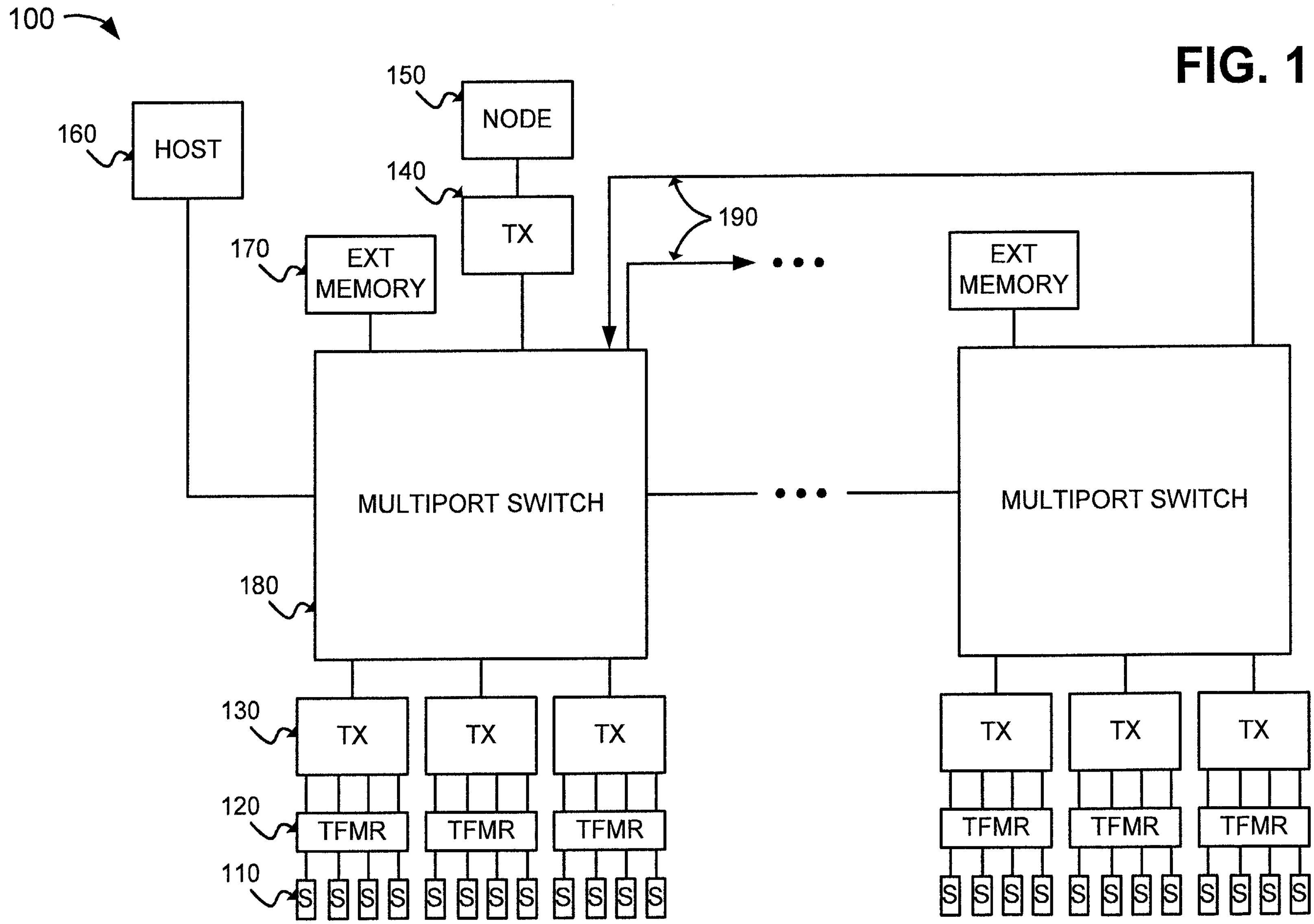
FIG. 1


100
HOST
160
150
NODE
140
TX
170
EXT
MEMORY
190
MULTIPORT SWITCH
180
TX
TFMR
S
130
120
110
EXT
MEMORY
MULTIPORT SWITCH

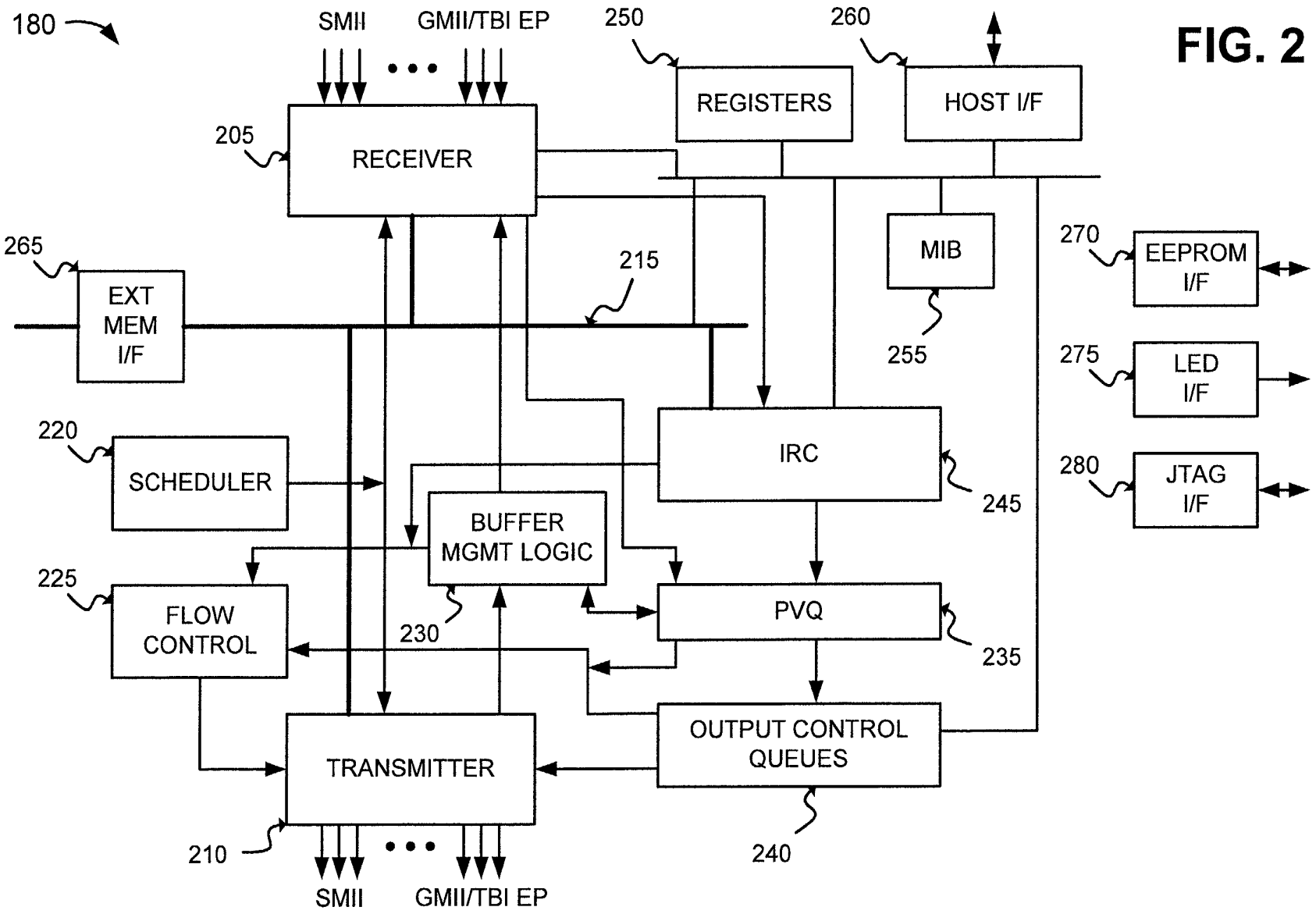

180
SMII
GMII/TBI EP
250
260
REGISTERS
HOST I/F
205
RECEIVER
265
EXT MEM I/F
215
MIB
255
270
EEPROM I/F
275
LED I/F
280
JTAG I/F
220
SCHEDULER
IRC
245
BUFFER MGMT LOGIC
225
FLOW CONTROL
230
PVQ
235
OUTPUT CONTROL QUEUES
TRANSMITTER
210
240
SMII
GMII/TBI EP

FIG. 2

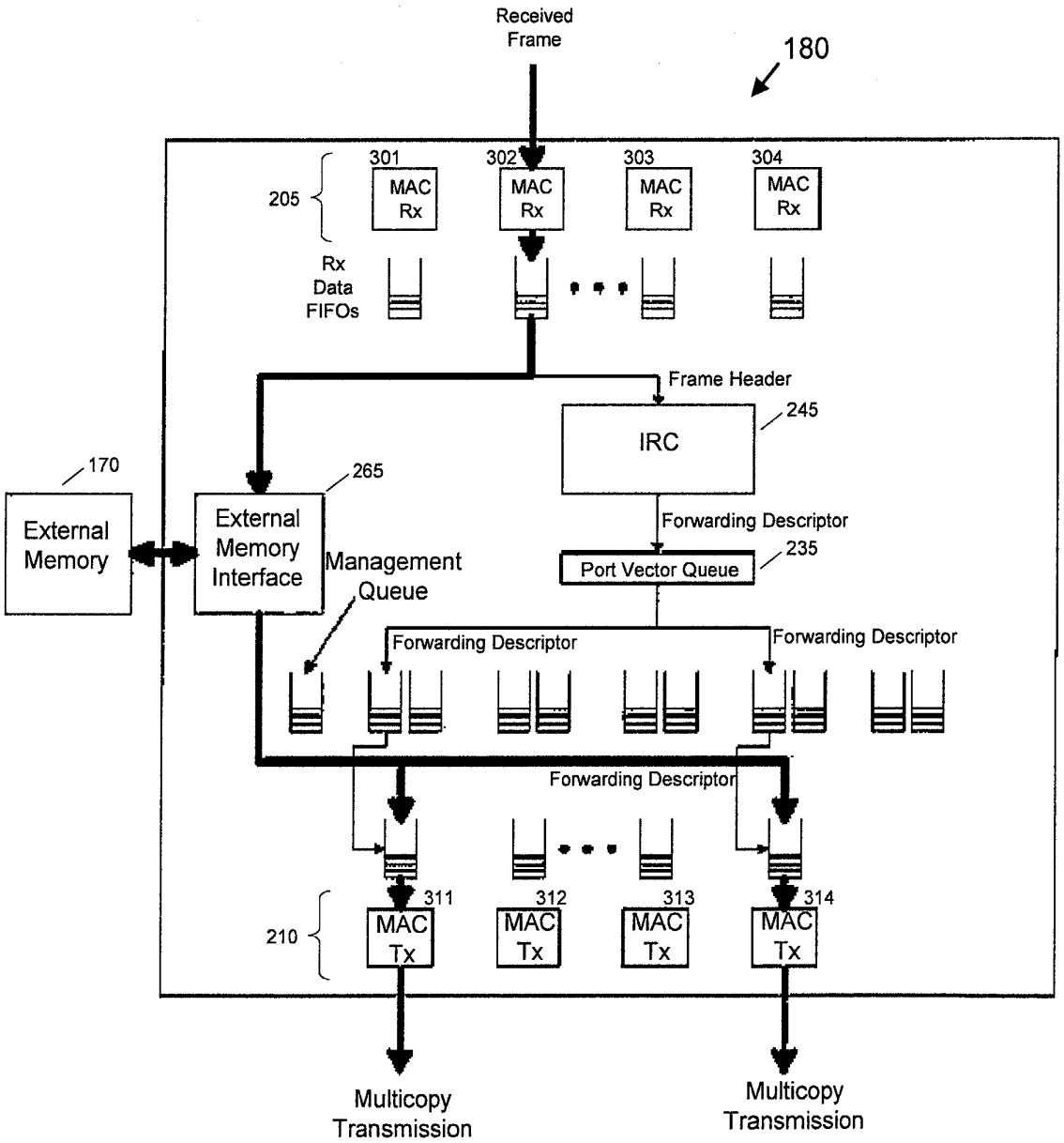

Received Frame
180
301
302
303
304
205
MAC Rx
MAC Rx
MAC Rx
MAC Rx
Rx Data FIFOs
Frame Header
IRC
245
170
265
External Memory
External Memory Interface
Management Queue
Forwarding Descriptor
Port Vector Queue
235
Forwarding Descriptor
Forwarding Descriptor
Forwarding Descriptor
311
312
313
314
210
MAC Tx
MAC Tx
MAC Tx
MAC Tx
Multicopy Transmission
Multicopy Transmission

Fig. 3

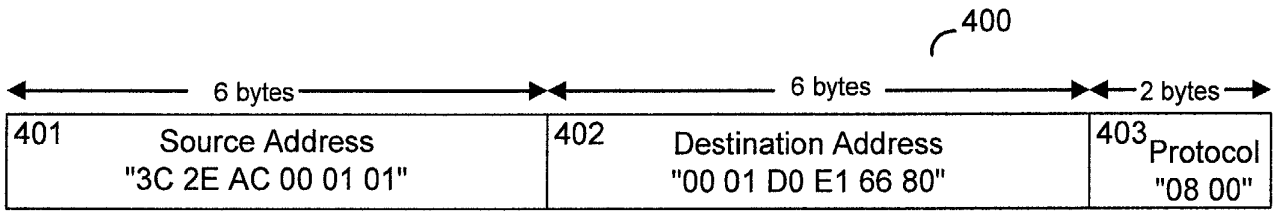

400
6 bytes
6 bytes
2 bytes
401
Source Address
"3C 2E AC 00 01 01"
402
Destination Address
"00 01 D0 E1 66 80"
403
Protocol
"08 00"

Fig. 4

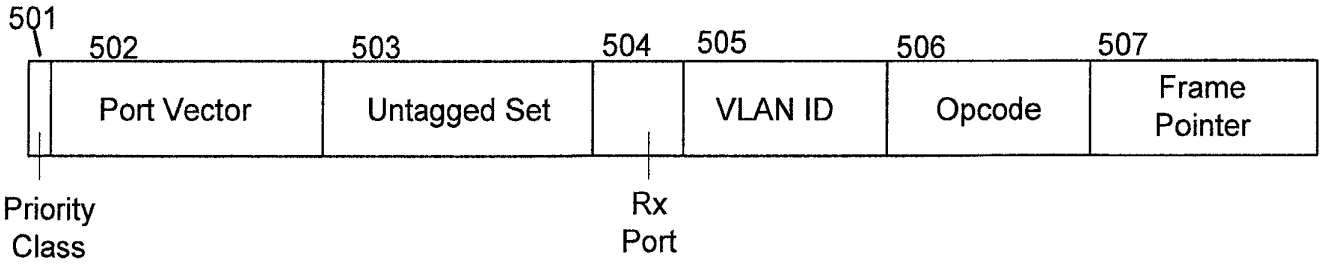

501
502
503
504
505
506
507
Port Vector
Untagged Set
VLAN ID
Opcode
Frame
Pointer
Priority
Class
Rx
Port

Fig. 5

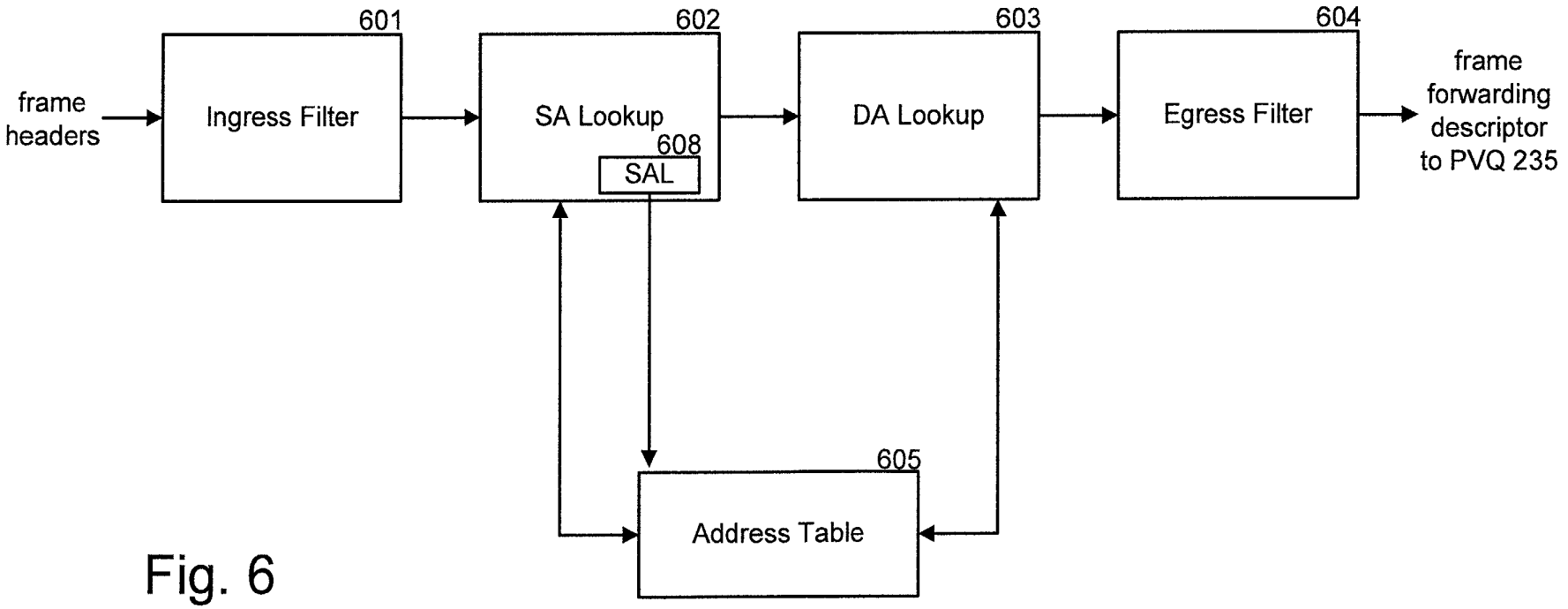


Fig. 6

245

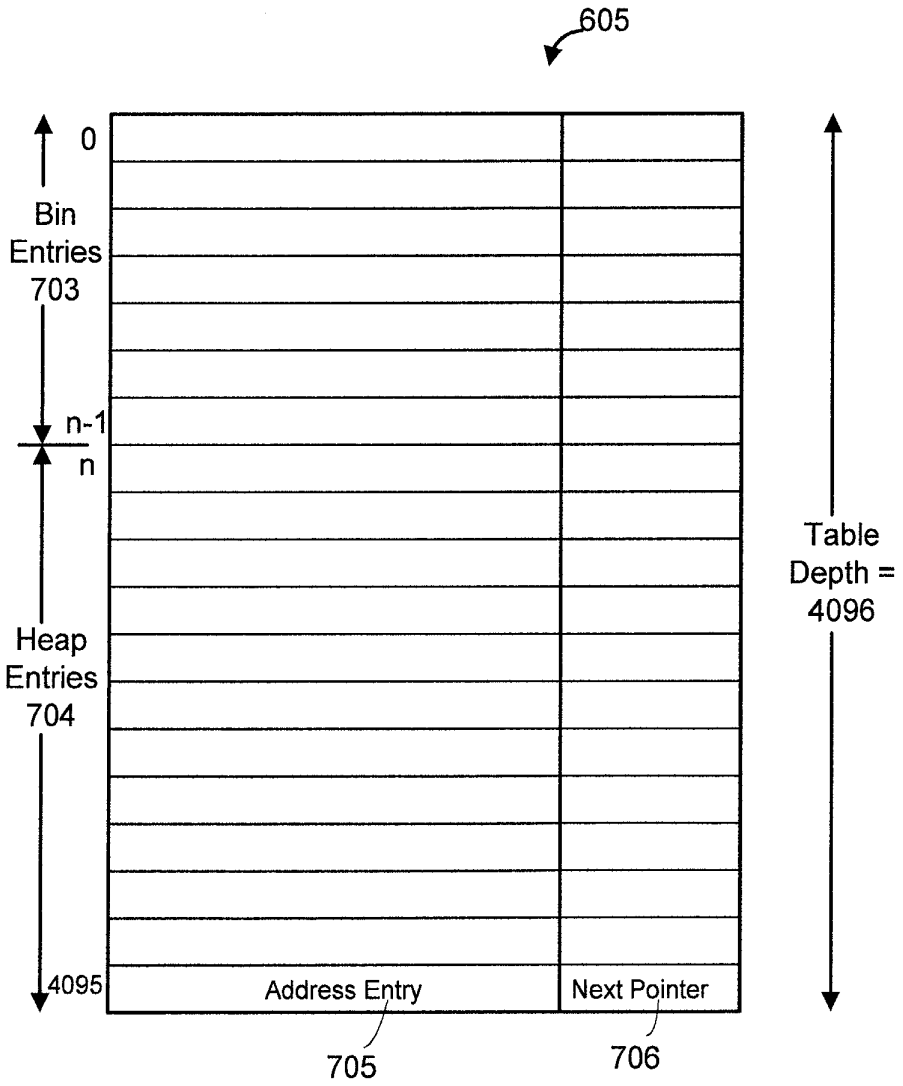

605
0
Bin
Entries
703
n-1
n
Heap
Entries
704
4095
Address Entry
Next Pointer
705
706
Table
Depth =
4096

Fig. 7

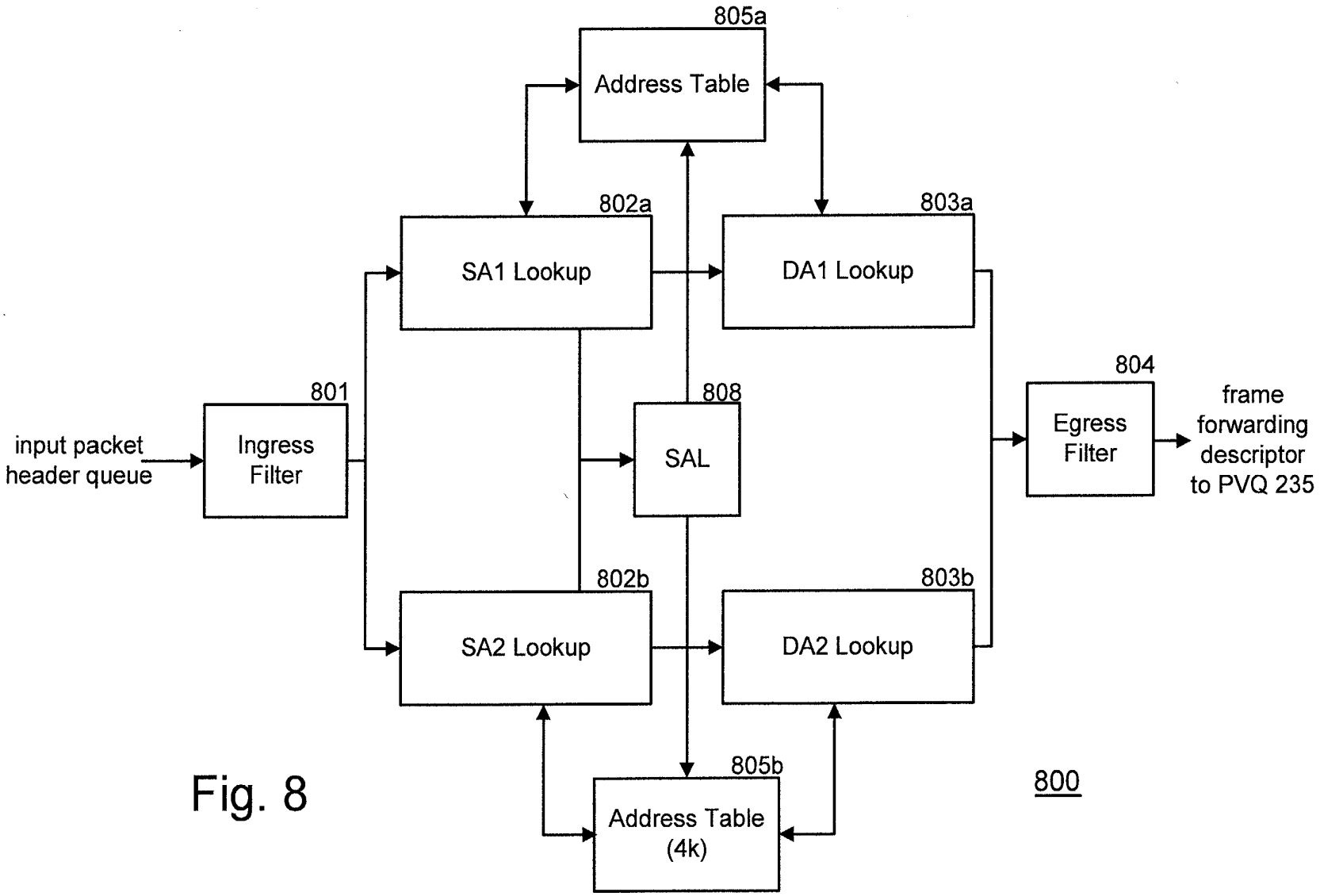

805a
Address Table
802a
SA1 Lookup
803a
DA1 Lookup
804
801
808
input packet
header queue
Ingress
Filter
SAL
Egress
Filter
frame
forwarding
descriptor
to PVQ 235
802b
803b
SA2 Lookup
DA2 Lookup
805b
Address Table
(4k)
800

Fig. 8

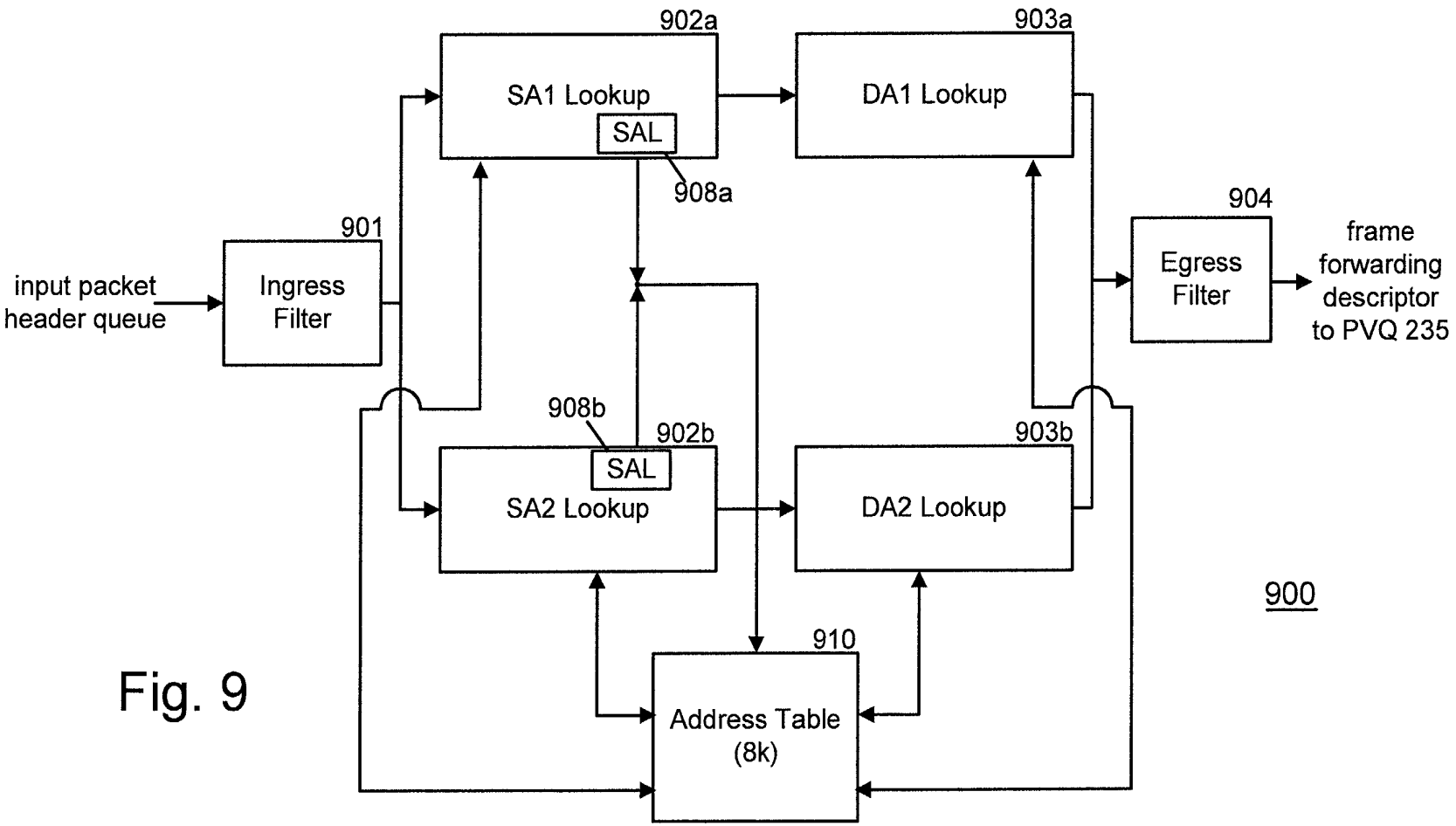

902a
SA1 Lookup
SAL
908a
903a
DA1 Lookup
904
Egress Filter
frame forwarding descriptor to PVQ 235
901
input packet header queue
Ingress Filter
908b
902b
SAL
SA2 Lookup
903b
DA2 Lookup
900
910
Address Table (8k)

Fig. 9